Electrical Performance of Annealed Zinc-Tin-Oxide Thin-Film Transistors Deposited by Atomic Layer Deposition (AGSR_100)

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Fabrication of devices on top of existing complimentary metal-oxide-semiconductor (CMOS) substrates is being studied as a way to increase device density and continue Moore's law. Zinc tin oxide (ZTO), an amorphous oxide semiconductor, is a strong candidate for heterointegration of thin film devices on CMOS owing to its wide bandgap (~3 eV), high electron mobility, and large area uniformity. Heterointegration of AOS on CMOS requires fabrication of high-performance devices using low temperature deposition techniques to preserve the underlying CMOS device performance. Among the potential candidate techniques, atomic layer deposition (ALD) is a promising low temperature thin film deposition process allowing precise control of film interface, stoichiometry, and thickness.

In this project, bottom-gate top contact thin film transistors (TFTs), as illustrated by the cross section in Figure 1, were fabricated with ALD ZTO thin films. The electrical properties of ZTO TFTs were studied as a function of annealing temperature and Zn:Sn ratio. The Zn:Sn ratio of the films was varied by changing the Zn:Sn ALD cycle ratio. X-ray photoelectron spectroscopy was used to study the Zn:Sn ratio and capture chemical composition changes with annealing. As an alternative to traditional patterning performed for device isolation via photolithography and etching, polymethyl methacrylate (PMMA) was studied as an ALD ZTO inhibition layer to enable additive manufacturing via area-selective ALD. In this way, a patterned layer of PMMA inhibits the growth of ZTO where present, depositing ZTO only in specified un-coated areas. This work presents a pathway towards scalable nanomanufacturing of electronics on a range of temperature-sensitive substrates.

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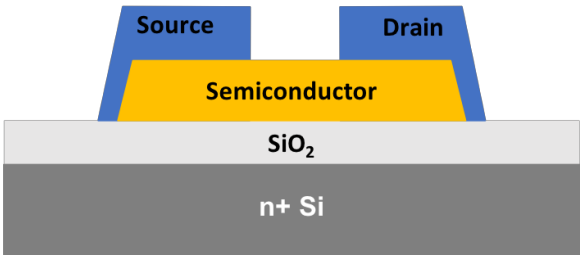

Figure 3: Cross section of bottom gate top contact TFT.